

IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Benjamin J. Patella, et al.

Confirmation No.:

Application No.:

Examiner:

Filing Date:

Group Art Unit:

Title: SYSTEM AND METHOD FOR EVALUATING THE SPEED OF A CIRCUIT

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

This Information Disclosure Statement is submitted:

- ☒ under 37 CFR 1.97(b), or
(Within three months of filing national application; or date of entry of national application; or before mailing date of first office action on the merits; whichever occurs last)
- ☐ under 37 CFR 1.97(c) together with either a:
☐ Statement under 37 CFR 1.97(e), or
☐ a \$180.00 fee under 37 CFR 1.17(p), or
(After the CFR 1.97 (b) time period, but before final action or notice of allowance, whichever occurs first)
- ☐ under 37 CFR 1.97 (d) together with a:
☐ Statement under 37 CFR 1.97(e)(1) or (2), and
☐ a \$180.00 fee set forth in 37 CFR 1.17(p).
(Filed after final action, a notice of allowance, on or before payment of the issue fee)

Please charge to Deposit Account **08-2025** the sum of \$0.00. At any time during the pendency of this application, please charge any fees required or credit any overpayment to Deposit Account **08-2025** pursuant to 37 CFR 1.25.

☒ Applicant(s) submit herewith Form PTO 1449 - Information Disclosure Citation together with copies, of patents, publications or other information of which applicant(s) are aware, which applicant(s) believe(s) may be material to the examination of this application and for which there may be a duty to disclose in accordance with 37 CFR 1.56.

☐ A concise explanation of the relevance of foreign language patents, foreign language publications and other foreign language information listed on PTO Form 1449, as presently understood by the individuals(s) designated in 37 CFR 1.56 (c) most knowledgeable about the content is given on the attached sheet, or where a foreign language patent is cited in a search report or other action by a foreign patent office in a counterpart foreign application, an English language version of the search report or action which indicates the degree of relevance found by the foreign office is listed on form PTO 1449 and is enclosed herewith.

It is requested that the information disclosed herein be made of record in this application.

"Express Mail" label no. **EV256031826US**

Date of Deposit **07-07-2003**

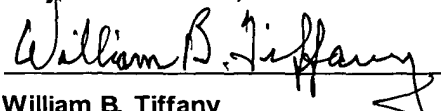
I hereby certify that this is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to: Commissioner for Patents, Washington, D.C. 20231.

By 

Typed Name: John Pallivathukal

Respectfully submitted,

Benjamin J. Patella, et al.

By 
William B. Tiffany

Attorney/Agent for Applicant(s)
Reg. No. **41,347**

Date: **07-07-2003**

PATENT APPLICATION

Sheet 1 of 1

<p>FORM PTO-1449</p> <p>LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT</p> <p>(Use several sheets if necessary)</p>	<p>ATTY. DOCKET NO. 200208752-1</p>	<p>APPLICATION NO.</p>	<p>CONFIRMATION NO.</p>
<p>APPLICANT Benjamin J. Patella, et al.</p>			
<p>FILING DATE</p>		<p>GROUP</p>	

REFERENCE DESIGNATION U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	PUBLICATION DATE	NAME	Pages, Columns, Lines Where Relevant Passages or Figures Appear
	1A	2002/0130695	09-19-2002	Jesephson et al.	
	1B	6,509,788	01-21-2003	Naffziger et al.	
	1C	6,489,834	12-03-2002	Naffziger et al.	
	1D				
	1E				
	1F				
	1G				
	1H				
	1I				
	1J				
	1K				

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	PUBLICATION DATE	NAME OF PATENTEE OR APPLICANT	Pages/Columns/Lines Where Relevant Passages/Figures Appear	Check if Translation attached
	1L					
	1M					
	1N					
	1O					
	1P					

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

	1Q	Dhar, S., et al., "Low-Power Digital Filtering Using Multiple Voltage Distribution and Adaptive Voltage Scaling," International Symposium on Low Power Electronic Design, (2000), pp. 207-209.
	1R	Chandrakasan, A., et al., "Design of High-Performance Microprocessor Circuits," IEEE Press, (2001), pp. 120, 128.
	1S	Kuroda, T., et al., "Variable Supply-Voltage Scheme for Low-Power High Speed CMOS Digital Design," IEEE Journal of Solid-State Circuits, Vol. 33, No. 3, (March 1998), pp. 454-462.

EXAMINER

DATE CONSIDERED